C64 DIAGNOSTIC INSTRUCTION AND TROUBLESHOOTING MANUAL ASSEMBLY #326070-01

TABLE OF CONTENTS

SECTION ONE

OPERATION AND TEST INSTRUCTIONS

SECTION TWO

BASIC TROUBLESHOOTING GUIDE

OPERATION AND TEST INSTRUCTIONS

1. UNPACKING

When you receive the C-64 Diagnostic Kit, it should include 1 each:

- Diagnostic Program Cartridge
- User Port Hardware Adapter
- Keyboard PCB
- Cable Harness Assembly
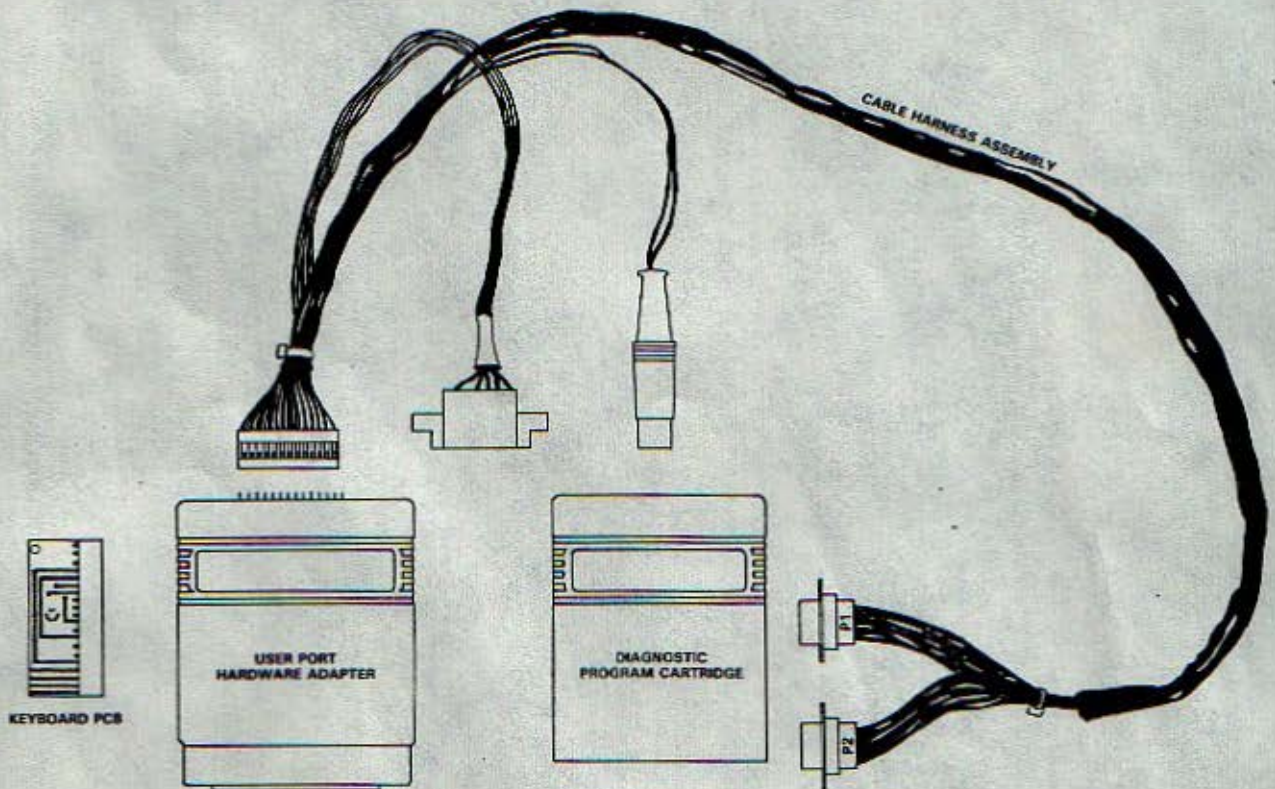
If any of these items are missing, please contact Commodore Parts Department.

2. BASIC DIAGNOSTIC THEORY

The Diagnostic Program Cartridge resides at location $8000-$9FFF. When the C-64 is turned on, memory locations $8004-$8008 are read. If these locations contain the characters CBM80, the program contained in the Diagnostic Cartridge is executed. The program exercises the 6510 MPU, system RAM, ROM and internal I/O circuits of the C-64. The test being executed, status (OK or BAD), and possible IC failure will be displayed.

3. INSTALLATION

3.1 Make sure the POWER is OFF on the C-64.

3.2 Plug the DIAGNOSTIC PROGRAM CARTRIDGE into the EXPANSION PORT.
- Make sure the label, C64 Diagnostic, is facing up.

3.3 Plug the CABLE HARNESS ASSEMBLY into the connector located on the back of the USER PORT HARDWARE ADAPTER.
- The connector is KEYED to allow it to be connected only one way. However, it is very easy to miss a row of pins, so care should be taken when connecting the harness.

3.4 Plug the USER PORT HARDWARE ADAPTER into the USER PORT.
- Make sure the LABEL AREA is facing UP. (Cartridge screw down.)

3.5 Plug the 6-PIN EDGE CONNECTOR into the CASSETTE PORT.
- The connector is KEYED to allow it to be plugged in only one way.

3.6 Plug the 6-PIN DIN CONNECTOR into the SERIAL PORT. (Disk drive port.)

3.7 Plug the 2 9-PIN MINI DIN CONNECTORS into the CONTROL PORTS.
- It makes no difference which connector goes to which port.

3.8 Check to make sure all connectors are installed correctly.
- The KEYBOARD PCB need NOT be connected to run the diagnostic.

3.9 Turn the POWER ON to the C-64.

4. OPERATION

The diagnostic test should 'Auto-Boot' on system power up and begin running the tests. If no screen is displayed, it is an indication that the system has an initial start-up problem. If this is the case, refer to the "Basic Troubleshooting Guide" in section 2.

If the C-64 executes the initial start-up sequence correctly, the current test being executed will be displayed. If an internal circuit fails the test, a 'BAD' message will be displayed next to the failed test and a probable IC failure is indicated inside the 'Red' rectangular box. If the internal circuit being tested passes the test, an 'OK' message is displayed next to the test.

It is possible to have a problem with the C-64 that is not a constant or hard failure. It may pass a test one time and fail the next. If a failure is detected, a 'BAD' message will be displayed in red next to the failed test and the probable IC failure will be indicated inside the 'Red' rectangular box. If the test passes on the next diagnostic cycle, the 'OK' message is displayed in red next to the test, and the probable IC failure indication will not be cleared from inside the box. This is an indication that a failure occurred at least once during diagnostic run time.

Once the diagnostic is running it will continue to execute, displaying the results of the tests, count (number of cycles run), and 2 time-of-day clocks. A detailed description of these clocks is contained in 5.17, LOWER SCREEN DISPLAY.

5. DIAGNOSTIC TEST DESCRIPTION

5.1 ZERO PAGE TEST

Zero page memory resides at locations $0000-$00FF. Two of these locations, $0000 and $0001, are reserved for the 6510 MPU I/O port. The zero page test writes Hex 00, 55, AA and FF into locations $0003-$00FF. The data is read and compared to stored data. If DATA READ = DATA STORED, zero page RAM is 'OK'. If DATA READ ≠ DATA STORED, zero page RAM is 'BAD'.

Zero page RAM is internal to the 6510 MPU; therefore, a zero page failure is probably due to a defective 6510 MPU, U7. If swapping U7 does not correct the problem, troubleshooting of the system power, reset, clocks, data bus and address bus will be necessary.

5.2 STACK PAGE TEST

The stack page resides at locations $0100-$01FF. The stack page test writes Hex 00, 55, AA and FF in locations $0100-01FF. The data is read and compared to stored data. If DATA READ = DATA STORED, stack page RAM is 'OK'. If DATA READ ≠ DATA STORED, stack page RAM is 'BAD'.

Stack page RAM is internal to the 6510 MPU; therefore a stack page failure is probably due to a defective 6510 MPU, U7. If swapping U7 does not correct the problem, troubleshooting of the system power, reset, clocks, data bus and address bus will be necessary.

5.3 SCREEN RAM TEST

The screen RAM resides at locations $0400-$07FF. The screen RAM test writes Hex 00, 55, AA and FF in locations $0400-$07FF. After a short delay, the data is read and compared to the written data. If DATA READ = DATA WRITTEN, screen RAM is 'OK'. If DATA READ ≠ DATA WRITTEN, screen RAM is 'BAD'.

Because the screen RAM is dynamic RAM, a refresh cycle must occur at least every 2 milliseconds. The program delay checks memory refreshing. If the screen RAM test fails, and only 1 RAM IC is displayed 'BAD', it is usually an indication of a stuck bit and the IC should be replaced. If multiple RAM IC's are displayed 'BAD', troubleshooting of the system user RAM area will be necessary.

• Refer to 5. SYSTEM RAM in the "Basic Troubleshooting Guide" •

5.4 RAM TEST 1

RAM test 1 does a memory test on locations $0800-$7FFF. RAM test 1 writes Hex 00, 55, AA and FF in locations $0800-$7FFF. After a refresh cycle occurs, the data is read and compared to written data. If DATA READ = DATA WRITTEN, RAM test 1 is 'OK'. If DATA READ ≠ DATA WRITTEN, RAM test 1 is 'BAD'.

If RAM test 1 fails and only 1 RAM IC is displayed 'BAD', it is usually an indication of a stuck bit and the IC should be replaced. If multiple RAM IC's are displayed 'BAD', troubleshooting of the system user RAM area will be necessary.

• Refer to 5. SYSTEM RAM in the "Basic Troubleshooting Guide" •

5.5 RAM TEST 2

RAM test 2 does a memory test on locations $3000-$FFFF. Before RAM test 2 is executed, the diagnostic program is transferred from $8000-$9FFF to $1000-$2FFF. RAM test 2 writes Hex 00, 55, AA, and FF into locations $3000-$FFFF. After a refresh cycle occurs, the data is read and compared to written data. If DATA READ = DATA WRITTEN, RAM test 2 is 'OK'. If DATA READ ≠ DATA WRITTEN, RAM test 2 is 'BAD'.

If RAM test 2 fails, and only 1 RAM IC is displayed 'BAD', it is usually an indication of a stuck bit and the IC should be replaced. If multiple RAM IC's are displayed 'BAD', troubleshooting of the system user RAM area will be necessary.

• Refer to 5. SYSTEM RAM in the "Basic Troubleshooting Guide" •

5.6 PLA TEST

The PLA, Programmable Logic Array, contains all the address decoding logic for system RAM, ROM and I/O. The PLA test reads the first byte of data from the Basic, Kernel and Character ROMS. The data is compared to stored values in the diagnostic cartridge. If DATA READ = DATA STORED, the PLA is able to select all ROMS. The PLA test then tests the I/O select output by reading one location of color RAM and comparing the data read to a stored value in the diagnostic cartridge. If the Basic ROM, Kernal ROM, Character ROM and Color RAM can all be selected, the PLA test is 'OK'.

If the PLA is displayed 'BAD' it should be replaced. If this does not correct the problem, troubleshooting of the system ROM and I/O circuitry will be necessary.

• Refer to 6. SYSTEM ROM AND I/O in the "Basic Troubleshooting Guide" •

5.7 COLOR RAM TEST

The color RAM resides at locations $D800-$DC00. The color RAM IC is a 1024 x 4 bit, 2114, static RAM chip. After storing the original color data on the stack, the color RAM test writes Hex 00, 05, 0A and 0F into locations $D800-$DC00, then reads it back. If DATA READ = DATA WRITTEN, color RAM is 'OK'. If DATA READ ≠ DATA WRITTEN, color RAM is 'BAD'.

If the color RAM test is 'BAD', the 2114 RAM IC, U6, should be replaced. If this does not correct the problem, troubleshooting of the associated circuitry will be necessary.

5.8 KERNAL, BASIC AND CHARACTER ROM TESTS

All operating system ROMS are checked by adding the contents of each address to a value equal to the sum of the data in all of the preceding addresses. This is referred to as a "Checksum". If the CALCULATED CHECKSUM = STORED CHECKSUM, the ROM being tested is 'OK'. If the CALCULATED CHECKSUM ≠ STORED CHECKSUM, the ROM being tested is 'BAD'.

If a ROM is defective, the 'BAD' message is displayed beside the ROM being tested. No IC will be displayed inside the 'Red' rectangular box.

The operating system ROMS are found at the following PCB locations:

Location U3 = Basic ROM
Location U4 = Kernal ROM
Location U5 = Character ROM

The diagnostic accurately checks all 3 versions of the Kernal ROM. If any ROM is displayed 'BAD', it should be replaced. If this does not correct the problem, troubleshooting of the system ROM and I/O circuitry will be necessary.

• Refer to 6. SYSTEM ROM AND I/O in the "Basic Troubleshooting Guide" •

5.9 CASSETTE PORT TEST

The cassette port test checks the cassette read and cassette sense inputs by outputting low pulses on the cassette sense line, which are read on the cassette read input. Cassette write and cassette motor outputs are checked by outputting low pulses on cassette motor, which are read on cassette write. If RECEIVED DATA = TRANSMITTED DATA, cassette port is 'OK'. If RECEIVED DATA ≠ TRANSMITTED DATA, cassette port is 'BAD'.

If the cassette port test fails, the indicated IC should be replaced. If this does not correct the problem, troubleshooting of the associated circuitry will be necessary.

5.10 KEYBOARD TEST

The keyboard matrix is scanned by a 6526 CIA, U1. During normal operation, 0 bits are output on port A, PA0-PA7. If a key is depressed, a 0 bit is returned on port B, PB0-PB7.

The keyboard test checks to see if the keyboard PCB is in place. If the connector is on, a binary count is output on port A, PA0-PA7. This binary count is looped through the connector and input on port B, PB0-PB7. The input count is read on port B, and compared to the output count on port A. If INPUT COUNT = OUTPUT COUNT, a binary count is output on port B, PB0-PB7. This binary count is looped through the connector and input on port A, PA0-PA7. The input count is read on port A, and compared to the output count on port B. If INPUT COUNT = OUTPUT COUNT, the keyboard is 'OK'. If INPUT COUNT ≠ OUTPUT COUNT, the keyboard is 'BAD'.

If the keyboard PCB is not in place, the keyboard test outputs 0 bits on port A, PA0-PA7, then reads port B, PB0-PB7. If Port B = 255, binary 11111111, the keyboard test displays 'OPEN', indicating no keys on the keyboard are depressed. If Port B ≠ 255, binary 11111111, the keyboard test displays 'BAD', indicating a 0 bit was detected on port B.

If the keyboard test displays 'BAD' or 'OPEN' with the keyboard PCB on, it usually indicates a defective 6526 CIA, U1. If the keyboard test displays 'BAD' with the keyboard PCB off, it usually indicates a shorted or depressed key on the keyboard.

** MAKE SURE THE SHIFT-LOCK KEY IS OFF **

If the keyboard is good, the 6526 CIA, U1, should be replaced. If this does not correct the problem, troubleshooting of the associated circuitry will be necessary.

5.11 CONTROL PORT TEST

The control port test checks both control ports, the joystick/paddle ports, by outputting signals on control port 1, JOYA0-JOYA3, then reading control port 2, JOYB0-JOYB3. The paddle inputs of both control ports, POTX-POTY, are tied to +5 VDC through 110K pull-up resistors, located on the user port hardware adapter.

The control port test checks the paddle inputs first. The 6581 SID IC, U18, converts the analog signal, developed across the 110K resistors, to a digital output. If this digital output falls within a specified range, the control port test continues.

The control port test checks the joystick and push button inputs by outputting zero bits on port A, PA0-PA4, and reading the input on port B, PB0-PB4. If PORT B INPUT = PORT A OUTPUT, the control port is 'OK'. If PORT B INPUT ≠ PORT A OUTPUT, the control port is 'BAD'.

If the control port test sees only paddle input 'BAD', it usually indicates a defective 4066 CMOS switch, U28, or 6526 CIA, U1. If both paddle inputs are detected 'BAO', it usually indicates a defective 6581 SID IC, U18, 4066 CMOS switch, U28, or 6526 CIA, U1.

If the control port displays 'BAD', any indicated IC should be replaced. If this does not solve the problem, troubleshooting of the associated circuitry will be necessary.

ON SOME OF THE OLDER 5-PIN VIDEO OUTPUT PCB's, THE CONTROL PORT WILL DISPLAY 'BAD' AND INDICATE A DEFECTIVE 6581 SID IC, U18, EACH TIME THE CONTROL PORT TEST RUNS. THIS IS DUE TO DIFFERENT VALUE CAPACITORS, PCB LOCATIONS C48 AND C93, AT PINS 23 AND 24 OF U1B, WHICH CAUSE THE DIGITAL OUTPUT TO FALL OUTSIDE OF THE SPECIFIED RANGE.

THESE CAPACITORS VALUES SHOULD BE 1800 PF. THIS SITUATION WILL NOT CAUSE ANY PROBLEMS WITH PADDLE OPERATION AND THESE CAPACITORS NEED NOT BE CHANGED IF A DIFFERENT VALUE CAP WAS USED AT THE TIME OF MANUFACTURE.

5.12 SERIAL PORT TEST

The serial port test checks the serial bus by generating an output signal on PA5, DATA OUT, of the 6526 CIA, U2, and reading PA7, DATA IN, and the FLAG input of the 6526 CIA, U1. If DATA IN ≠ DATA OUT, serial port is 'BAD'. If DATA IN = DATA OUT, the serial port test continues.

An output signal is generated on PA3, ATN OUT, of the 6526 CIA, U2, and read on PA6, CLK IN. An output signal is then generated on PA4, CLK OUT, of the 6526 CIA, U2, and read on PA6, CLK IN. If DATA IN = DATA OUT, serial port is 'OK'. If DATA IN ≠ DATA OUT, serial port is 'BAD'.

If the serial port displays 'BAD', any indicated IC should be replaced. If this does not correct the problem, troubleshooting of the associated circuitry will be necessary.

5.13 USER PORT TEST

The user port test checks the C-64 user port by generating an output signal on PA3, ATN OUT, of the 6526 CIA, U2, and reading the input on PA2. If DATA IN ≠ DATA OUT, the user port is 'BAD'. If DATA IN = DATA OUT, the user port test continues.

A binary count is output on PB0-PB3 of the 6526 CIA, U2, and read on PB4-PB7. If DATA IN ≠ DATA OUT, the user port is 'BAD'. If DATA IN = DATA OUT, the user port test continues.

An output signal is generated on PC2 and read on FLAG 2. If DATA IN ≠ DATA OUT, the user port is 'BAD'. If DATA IN = DATA OUT, the user port test continues.

An output signal is generated on SP1 and read on SP2. If DATA IN ≠ DATA OUT, the user port is 'BAD'. If DATA IN = DATA OUT, the user port test continues.

An output signal is generated on SP2 and read on SP1. If DATA IN = DATA OUT, the user port is 'OK'. If DATA IN ≠ DATA OUT, the user port is 'BAD'.

If the user port displays 'BAD', any indicated IC should be replaced. If this does not correct the problem, troubleshooting of the associated circuitry will be necessary.

5.14 TIMER 1-A/1-B — TIMER 2-A/2-B TEST

The timer tests check the internal clocks of the 6526 CIA's U1 and U2, by setting up the timer pointers and 6526 CIA addresses to be utilized. The timers are set to run at 60HZ, derived from the TOD inputs on pin 19 of the 6526 CIA's, U1 and U2. The timers continue to run until the interrupts are sensed. If the interrupts are sensed within, (23 * 256 + 16), 6510 clock cycles, the timers are 'OK'. If the interrupts are not sensed, the timers are 'BAD'.

If the timer tests are displayed 'BAD', it is necessary to watch for the status of the interrupt test. The following applies:

Timer 1(A/B)	Timer 2(A/B)	Interrupt	6510 (U7)	6526 CIA(U1)	6526 CIA(U2)
OK	OK	OK	OK	OK	OK
BAD	OK	OK	OK	BAD	OK
OK	BAD	OK	OK	OK	BAD
OK	OK	BAD	BAD	OK	OK
BAD	BAD	BAD	BAD	OK	OK

If this does not correct the problem, troubleshooting of the associated circuitry will be necessary.

5.15 INTERRUPT TEST

The interrupt test checks the internal timers of the 6526 CIA's U1 and U2, using the IRQ and NMI vectors. If an interrupt is not sensed on the IRQ of the 6526 CIA, U1, or the NMI of the 6526 CIA, U2, the interrupt is 'BAD'. If both interrupts are sensed, the interrupt test continues.

The internal alarms of the 6526 CIA's, U1 and U2, are tested by adding 2 seconds to the clock and waiting for the alarm interrupt to go off. If the alarm interrupt is not sensed, the interrupt is 'BAD'. If the alarm interrupt is sensed, the interrupt test continues.

The data line interrupt is tested by outputting on the 6526 CIA, U1, and waiting for an interrupt to occur on the 6526 CIA, U2. Data is then output on the 6526 CIA, U2, and a check is done for an interrupt to occur on the 6526 CIA, U1. If the interrupts occur, the interrupt is 'OK'. If an interrupt is not sensed, the interrupt is 'BAD'.

If the interrupt displays 'BAD', refer to the failure chart in section 5.14. If this does not correct the problem, troubleshooting of the associated circuitry will be necessary.

5.16 SOUND TEST

The sound test is an audible test ONLY and no 'OK' or 'BAD' message will be displayed. The sound test should produce 3 distinctive voices at 3 volume levels followed by 3 bursts of noise.

If any of the voices, volume levels or noise bursts are missing, it indicates a defective 6581 SID IC, U18. If replacement of the SID IC does not correct the problem, troubleshooting of the associated circuitry will be necessary.

5.17 LOWER SCREEN DISPLAY

During diagnostic run time, the diagnostic displays the number of cycles completed, COUNT, in the bottom left hand corner of the screen.

In the bottom right hand corner of the screen, the 2 clocks are displayed. The AM clock corresponds to the internal time-of-day clock of the 6526 CIA, U1, and the PM clock corresponds to the internal time-of-day clock of the 6526 CIA, U2.

The 2 clocks should show the **EXACT SAME TIME** during diagnostic run time and increment as the diagnostic tests are run. The increments of the clocks are as follows:

Current Test	AM Clock	PM Clock	Current Test	AM Clock	PM Clock
Zero Page	00:00:00	00:00:00	Cassette	00:00:24	00:00:24
Stack Page	00:00:00	00:00:00	Keyboard	00:00:24	00:00:24
Screen RAM	00:00:00	00:00:00	Control Port	00:00:24	00:00:24
Ram Test 1	00:00:11	00:00:11	Serial Port	00:00:24	00:00:24
Ram Test 2	00:00:15*	00:00:15	Timer 1 A	00:00:24	00:00:24
PLA Test	00:00:24	00:00:24	Timer 1 B	00:00:24	00:00:24
Color RAM	00:00:24	00:00:24	Timer 2 A	00:00:24	00:00:24
Kernal ROM	00:00:24	00:00:24	Timer 2 B	00:00:24	00:00:24
Basic ROM	00:00:24	00:00:24	Interrupt	00:00:37	00:00:37
Character ROM	00:00:24	00:00:24	Alarm Set	00:00:39**	00:00:39
			Sound Test	00:00:41	00:00:41
			New Cycle	00:00:58***	00:00:58

Failure modes:
Incorrect AM Clock — Possible 6526 CIA (U1) Failure
Incorrect PM Clock — Possible 6526 CIA (U2) Failure
Incorrect Both Clocks — Possible 60HZ TOD Input Failure

*   May vary between 00:00:15 thru 00:00:16
**   Alarm set does not display on the screen
*** Beginning of the 2nd cycle

C-64 BASIC TROUBLESHOOTING GUIDE

BASIC PRELIMINARY CHECKS

There are a few basic checks which should be made on the C-64 when troubleshooting a system with NO VIDEO ON POWER-UP. Although there are several things which may cause this symptom, these preliminary checks will eliminate some of the more common failures. If all of these basic areas seem correct, more advanced checks are covered in SECTIONS 1 through 7. In order to separate these checks by category, the following symbols are used prior to the step number in each section:

      B Basic System Checks

      A Advanced System Checks

      P Signals on System Power Up

ALL SIGNALS ARE TAKEN WITH THE DIAGNOSTIC CARTRIDGE INSTALLED

ALL MEASUREMENTS ARE WITHIN A +/−10% TOLERANCE

ALL READINGS ARE TAKEN WITH AN OSCILLOSCOPE

B PRE-CHECK 1   Measure the +5 VDC signal on pin 24 of IC U5.
                        • Result = +5 VDC   — Continue to PRE-CHECK 2

B PRE-CHECK 2   Measure the +5 VDC CAN signal on pin 40 of IC U19.
                        • Result = +5 VDC   — Continue to PRE-CHECK 3

B PRECHECK 3   Measure the +12 VDC signal on pin 13 of IC U19.
                        • Result = +12 VDC   — Continue to PRE-CHECK 4

If a result is incorrect, refer to 1. SYSTEM POWER SUPPLY.

P PRE-CHECK 4   Measure the RESET signal on pin 40 of IC U7.
                        • Result = 0 VDC on System Power Up to
                                  +5 VDC in Approximately 1 Second — Continue to PRE-CHECK 5

If the result is incorrect, refer to 2. SYSTEM RESET.

B PRE-CHECK 5   Measure the φCOLOR signal on pin 21 of IC U19.
                        • Result = 14.3 MHZ Clock   — Continue to PRE-CHECK 6

B PRE-CHECK 6   Measure the φIN signal on pin 22 of IC U19.
                        • Result = 8.18 MHZ Clock   — Continue to PRE-CHECK 7

B PRE-CHECK 7   Measure the φ0IN signal on pin 1 of IC U7.
                        • Result = 1.0 MHZ Clock   — Continue to PRE-CHECK 8

B PRE-CHECK 8   Measure the $\phi2$ signal on pin 39 of IC U7.
- Result = 1.0 MHZ Clock   — Continue to PRE-CHECK 9

If a result is incorrect, refer to 3. SYSTEM CLOCKS.

B PRE-CHECK 9   Measure the COMPOSITE signal on pin 4 of connector CN5.
- Result = Approximately +2 VDC Composite — Continue to PRE-CHECK 10

B PRE-CHECK 10   Measure the LUMINANCE signal on pin 1 of connector CN5.
- Result = Approximately +1 VDC Luminance — Continue to PRE-CHECK 11

B PRE-CHECK 11   Measure the COLOR signal on pin 6 of connector CN5.
- Result = Approximately +1 VDC Color   — Continue to 5. SYSTEM RAM.

If a result is incorrect, refer to 4. SYSTEM VIDEO.

All the signals listed, PRELIMINARY CHECKS 1 THRU 11, must be present for the system to produce the correct video display. If they seem correct, begin the **B** , BASIC, steps in 5. SYSTEM RAM.

> FOR FASTER TROUBLESHOOTING OF THE SYSTEM, CHECK ONLY THE STEPS IN THE
> SECTIONS MARKED AS BASIC, **B** , OR POWER UP, **P** , UNTIL A PROBLEM IS
> DETECTED. ONCE A PROBLEM IS DISCOVERED, CONTINUE TO THE ADVANCED, **A** ,
> CHECKS OF THE SECTION.

1. SYSTEM POWER SUPPLY

This section covers procedures for troubleshooting the C-64 power supply circuits. When
referring to this section, it is assumed that from the "Preliminary Basic Checks 1-3", there is a
problem with one or more of the +5 VDC CAN, +5 VDC or +12 VDC supplies.

1.1 — INCORRECT +5 VDC CAN SUPPLY

B STEP 1   Measure the output signal on pin 2 of voltage regulator VR2.
  - Result = +5 VDC   — Supply OK, Open Trace
  - Result = Incorrect   — Continue to Step 2

B STEP 2   Measure the input signal on pin 1 of voltage regulator VR2.
  - Result = +9 to +12 VDC   — Defective VR2
  - Result = Incorrect   — Continue to Step 3

B STEP 3   Measure the AC IN signal on pins 4 and 6 of rectifier CR4.
  - Result = Both 9 to 12 VAC   — Defective CR4
  - Result = Pin 4 Incorrect   — Continue to Step 4
  - Result = Pin 6 Incorrect   — Continue to Step 5
  - Result = Both Incorrect   — Continue to Step 4

B STEP 4   Measure the AC IN signal on pin 6 of connector CN7.
  - Result = 9 to 12 VAC   — Defective L4, SW1
  - Result = Incorrect   — Defective Power Supply

B STEP 5   Measure the AC IN signal on pin 7 of connector CN7.
  - Result = 9 to 12 VAC   — Defective L4, F1
  - Result = Incorrect   — Defective Power Supply

1.2 — INCORRECT +12 VDC SUPPLY

B STEP 6   Measure the output signal on pin 2 of voltage regulator VR1.
  - Result = +12 VDC   — Supply OK, Open Trace
  - Result = Incorrect   — Continue to Step 7

B STEP 7   Measure the input signal on pin 1 of voltage regulator VR1.
  - Result = +15 to +18 VDC   — Defective VR1
  - Result = Incorrect   — Continue to Step 8

B STEP 8   Measure the signal at the anode of diode CR6.
  - Result = 9 to 12 VAC Riding on a
              +9 to +12 VDC Level   — Defective CR5
  - Result = 9 to 12 VAC Only   — Defective CR6
  - Result = +9 to +12 VDC Only   — Problem with +5 VDC CAN Supply
                                           Refer to Step 1

1.3 — INCORRECT +5 VDC SUPPLY

B STEP 9   Measure the signal on the + side of capacitor C91.
  • Result = +5 VDC   — Supply OK, Open Trace
  • Result = Incorrect   — Continue to Step 10

B STEP 10   Measure the +5 VDC signal on pin 5 of connector CN7.
  • Result = +5 VDC   — Defective L5, SW1
  • Result = Incorrect   — Defective Power Supply

2. SYSTEM RESET

This section covers procedures for troubleshooting the C-64 RESET circuits. When referring to this section, it is assumed from the basic preliminary check, PRE-CHECK 4, that there is a problem with the system RESET.

2.1 — INCORRECT SYSTEM RESET

B STEP 1   Measure the output signal on pin 9 of IC U20.
  • Result = +5 VDC on System
  Power Up to 0 VDC in approximately
  1 second   — Continue to Step 2
  • Result = Incorrect   — Defective U20, C24, C105, R34

B STEP 2   Measure the RESET signal on pin 40 of IC U7.
  • Result = 0 VDC on System
  Power up to +5 VDC in
  approximately 1 Second   — Reset OK, Open Trace
  • Result = Incorrect   — Defective U8, U7

3. SYSTEM CLOCKS

This section covers procedures for troubleshooting the C-64 CLOCK circuits. When referring to this section, it is assumed from the basic preliminary checks, PRE-CHECK 5-8, that there is a problem with one, or more, of the 1 MHZ, 14.3 MHZ, or 8.18 MHZ system clocks.

3.1 — INCORRECT SYSTEM CLOCKS

B STEP 1   Measure the input signal on pin 13 of IC U31.
  • Result = 14.3 MHZ Clock   — Continue to Step 2
  • Result = Incorrect   — Defective Y1, U31

B STEP 2   Measure the input signal on pin 21 of IC U19.
  • Result = 14.3 MHZ Clock   — Continue to Step 3
  • Result = Incorrect   — Defective U31, U30, U19, FB16

B STEP 3   Measure the input signal on pin 11 of IC U29.
  • Result = 2.0 MHZ Clock   — Continue to Step 4
  • Result = Incorrect   — Defective U30, U29

B STEP 4 Measure the input signal on pin 1 of IC U32.
- Result = 1.0 MHZ Clock — Continue to Step 5
- Result = Incorrect — Defective U29, U32

B STEP 5 Measure the input signal on pin 1 of IC U7.
- Result = 1.0 MHZ Clock — Continue to Step 6
- Result = Incorrect — Defective U19, U7, U32

B STEP 6 Measure the signal on the BASE of transistor Q7.
- Result = +2 to +3 VDC — Continue to Step 7
- Result = Incorrect — Defective U32, Q7

B STEP 7 Measure the input signal on pin 9 of IC U32.
- Result = +1.5 to +2 VDC — Continue to Step 8
- Result = Incorrect — Defective Q7, U32

B STEP 8 Measure the input signal on pin 2 of IC U31.
- Result = +2 to +3 VDC — Continue to Step 9
- Result = Incorrect — Defective U32, U31

B STEP 9 Measure the input signal on pin 22 of IC U19.
- Result = 8.18 MHZ Clock — Continue to Step 10
- Result = Incorrect — Defective U31, U19, FB17

B STEP 10 Measure the output signal on pin 39 of IC U7.
- Result = 1.0 MHZ Clock — Clocks OK
- Result = Incorrect — Defective U18, U7, U1, U2

3.2 — INCORRECT SYSTEM CLOCKS   C-64 REVISION B — PCB ONLY

B STEP 1 Measure the input signal on pin 13 of IC U31.
- Result = 14.3 MHZ Clock — Continue to Step 2
- Result = Incorrect — Adjust CT1 — Defective Y1, U31

B STEP 2 Measure the input signal on pin 21 of IC U19.
- Result = 14.3 MHZ Clock — Continue to Step 3
- Result = Incorrect — Defective U31, U19

B STEP 3 Measure the input signal on pin 22 of IC U19.
- Result = 8.18 MHZ Clock — Continue to Step 4
- Result = Incorrect — Defective U31, U19

B STEP 4 Measure the input signal on pin 1 of IC U7.
- Result = 1.0 MHZ Clock — Continue to Step 5
- Result = Incorrect — Defective U19, U7

B STEP 5 Measure the output signal on pin 39 of IC U7.
- Result = 1.0 MHZ Clock — Clocks OK
- Result = Incorrect — Defective U18, U7, U1, U2

4. SYSTEM VIDEO

This section covers procedures for troubleshooting the C-64 VIDEO circuits. When referring to this section, it is assumed from the basic preliminary checks, PRE-CHECK 9-11, that there is a problem with one or more of the video outputs.

THESE SIGNALS MAY CAUSE A "NO VIDEO" OR "INCORRECT VIDEO" SYMPTOM

4.1 — INCORRECT SYSTEM VIDEO

B STEP 1 Measure the SYNC/LUM signal on pin 15 of IC U19.
- Result = +5 VDC Composite   — Continue to Step 4
- Result = Incorrect   — Continue to Step 2

P STEP 2 Measure the C/S signal on pin 10 of IC U19.
- Result = +5 VDC with a
  Negative Pulse ONCE
  on system Reset   — Continue to Step 3
- Result = Incorrect   — Defective U19, U17, U15

P STEP 3 Measure the R/W signal on pin 11 of IC U19.
- Result = +5 VDC with a
  negative Pulse ONCE
  on system Reset   — Defective U19, M1
- Result = Incorrect   — Defective U19, U17, U7, U6, U1,
  U2, U9-U12, U21-U24

B STEP 4 Measure the COLOR signal on pin 14 of IC U19.
- Result = +2 VDC Color on a
  +5 to +6 VDC Level   — Continue to Step 5
- Result = Incorrect   — Defective U19, M1

A STEP 5 Measure the COMPOSITE signal on pin 4 of connector CN5.
- Result = +2 VDC Composite   — Continue to Step 6
- Result = Incorrect   — Defective M1

A STEP 6 Measure the LUMINANCE signal on pin 1 of connector CN5.
- Result = +1 VDC Sync/Lum   — Continue to Step 7
- Result = Incorrect   — Defective M1

A STEP 7 Measure the COLOR signal on pin 6 of connector CN5.
- Result = +1 VDC Color   — Video OK
- Result = Incorrect   — Defective M1

5. SYSTEM RAM

This section covers procedures for troubleshooting the C-64 user RAM area. Bad RAM IC's are a common problem when the system does not produce a screen on "Power-Up". It is not uncommon to have more than 1 RAM IC failure.

```
SEVERAL RAM IC's FOUND DEFECTIVE MAY INDICATE A BAD POWER SUPPLY
```

5.1 — SYSTEM RAM CIRCUITRY

B STEP 1   With power applied to the system, feel IC's U9-U12, U21-U24.
- Result = No IC's feel HOT — Continue to Step 2
- Result = One or More IC's
  Feels EXTREMELY HOT — Replace Hot IC's

P STEP 2   Measure the DATA signal on pin 2 of each IC U9-U12, U21-U24. These DATA signals **MUST GO TO A STRONG +5 VDC LEVEL IMMEDIATELY** when power is applied to the system.
- Result = Strong +5 VDC Data
  Immediately on Power Up — Continue to Step 3
- Result = Slow or Incorrect — Defective U9-U12, U21-24

B STEP 3   Measure the CASRAM signal on pin 15 of IC's U9-U12, U21-U24.
- Result = +5 VDC Pulse — Continue to Step 4
- Result = Incorrect — Continue to Step 3.1

A STEP 3.1   Cut pin 18, CASRAM, of IC U17 and measure the signal on CUT PIN.
- Result = +5 VDC Pulse — Defective U9-U12, U21-U24
- Result = Incorrect — Defective U17

P STEP 4   Measure the R/W signal on pin 3 of IC's U9-U12, U21-U24.
- Result = +5 VDC with a
  Negative Pulse ONCE
  on system Reset — Continue to Step 5
- Result = Incorrect — Defective U9-U12, U21-U24,
  U17, U7, U1, U2

B STEP 5   Measure the RAS signal on pin 4 of IC's U9-U12, U21-U24.
- Result = +2 VDC Pulse — Continue to Step 6
- Result = Incorrect — Defective U9-U12, U21-U24,
  U19, U26

A STEP 6   Measure the output signal on pins 1, 7, 9, 12 of IC U13.
- Result = +5 VDC Pulse — Continue to Step 8
- Result = Incorrect — Continue to Step 7

A STEP 7   Measure the input signal on pins 2, 3, 5, 6, 10, 11, 13, 14 of IC U13.
- Result = +5 VDC Pulse   — Continue to Step 7.1
- Result = Incorrect   — Continue to Step 7.3

A STEP 7.1 Measure the C/S ENABLE signal on pins 1, 15 of IC U13.
- Result = +5 VDC Pulse   — Continue to Step 7.2
- Result = Incorrect Pin 1   — Defective U17, U19, U14, U13, U25
- Result = Incorrect Pin 15   — Defective U17, U19, U14, U13, U25, U26, U27, U6, U8

A STEP 7.2 Cut pin 8, +5 VDC, of IC U9-U12 and U21-U24 one at a time and measure the incorrect signal from Step 6 after each cut.
- Result = +5 VDC Pulse   — Defective U9-U12, U21-U24
- Result = Incorrect   — Defective U13

A STEP 7.3 If incorrect signal of IC U13 from Step 7 is on:
- Pin 2, 5, 11, 14   — Defective U17, U13, U7
- Pin 3, 6, 10, 13   — Continue to Step 7.4

A STEP 7.4 Cut pin 24, +5 VDC, of IC's U3, U4, U5 one at a time and measure the incorrect signal from Step 7.3 after each cut.
- Result = +5 VDC Pulse   — Defective U3, U4, U5
- Result = Incorrect   — Defective U25, U7, U26, U6

B STEP 8   Measure the output signal on pins 4, 7, 9, 12 of IC U25.
- Result = +5 VDC Pulse   — Continue to 6. SYSTEM ROM AND I/O
- Result = Incorrect   — Continue to Step 9

A STEP 9   Measure the input signal on pins 2, 3, 5, 6, 10, 11, 13, 14 of IC U25.
- Result = +5 VDC Pulse   — Continue to Step 9.1
- Result = Incorrect   — Continue to Step 9.2

A STEP 9.1 Cut pin 8, +5 VDC, of IC's U9-U12, U21-U24 one at a time and measure the incorrect signal from Step 8 after each cut.
- Result = +5 VDC Pulse   — Defective U9-U12, U21-U24
- Result = Incorrect   — Defective U25

A STEP 9.2 Cut pin 24, +5 VDC, of IC's U3, U4, U5 one at a time and measure the incorrect signal from Step 9 after each cut.
- Result = +5 VDC Pulse   — Defective U3, U4, U5
- Result = Incorrect on Pin 3, 6, 10, 13   — Defective U25, U7, U26, U6, U1, U2
- Result = Incorrect on Pin 2, 5, 11, 14   — Defective U25, U7, U26, U6

6. SYSTEM ROM AND I/O

This section covers procedures for troubleshooting the C-64 ROM Selection and I/O Decoding. This area is a common problem when the system does not produce a screen on System Power Up.

6.1 — SYSTEM ROM SELECTION AND I/O DECODING

P   STEP 1   Measure the CHAR ROM SELECT signal on pin 15 of IC U17.
- **Result = +5 VDC with
  Negative Pulse**   — Continue to Step 2
- **Result = Incorrect**   — Defective U17, U5

P   STEP 2   Measure the KERN ROM SELECT signal on pin 16 of IC U17.
- **Result = +5 VDC with
  Negative Pulse**   — Continue to Step 3
- **Result = Incorrect**   — Defective U17, U4

P   STEP 3   Measure the BASIC ROM SELECT signal on pin 17 of IC U17.
- **Result = +5 VDC with
  Negative Pulse on system
  Reset**   — Continue to Step 4
- **Result = Incorrect**   — Defective U17, U3

B   STEP 4   Measure the I/O ENABLE signal on pin 12 of IC U17.
- **Result = +5 VDC with
  Negative Pulse**   — Continue to Step 5
- **Result = Incorrect**   — Defective U17, U15

B   STEP 5   Measure ADDRESSES 12-15 on pins 2, 3, 4, 27 of IC U17.
- **Result = +5 VDC Pulse**   — Continue to Step 6
- **Result = Incorrect**   — Defective U17, U7, U13, U26,
                                                    U27, U6, U8

A   STEP 6   Measure the CHAREN, HIRAM, LORAM signals on pins 6, 7, 8 of IC U17.
- **Result = +5 VDC Pulse**   — Continue to Step 7
- **Result = Incorrect**   — Defective U17, U7

A   STEP 7   Measure the ROM L signal on pin 11 of IC U17.
- **Result = +5 VDC Pulse**   — Continue to Step 8
- **Result = Incorrect**   — Defective U17, Cartridge

A   STEP 8   Measure the CASRAM signal on pin 18 of IC U17.
- **Result = +5 VDC Pulse**   — Continue to Step 9
- **Result = Incorrect**   — Continue to Step 8.1

A   STEP 8.1 Cut pin 18, CASRAM, of IC U17 and measure the signal on the cut pin.
- **Result = +5 VDC Pulse**   — Defective U9-U12, U21-U24
- **Result = Incorrect**   — Defective U17

A STEP 9   Measure VA12, VA13 on pins 20, 21 of IC U17.
           • Result = +5 VDC Pulse   — Continue to Step 10
           • Result = Incorrect   — Defective U17, U19, U26, U9-U12,
                                               U21-U24

A STEP 10   Measure the EXROM signal on pin 23 of IC U17.
           • Result = 0 VDC   — Continue to Step 11
           • Result = Incorrect   — Defective U17, Cartridge

P STEP 11   Measure the R/W signal on pin 24 of IC U17.
           • Result = +5 VDC with
             Negative Pulse ONCE
             on system Reset   — Continue to Step 12
           • Result = Incorrect   — Defective U17, U21, U9-U12,
                                               U21-24

A STEP 12   Measure the AEC signal on pin 25 of IC U17.
           • Result = +5 VDC Pulse   — Continue to Step 13
           • Result = Incorrect   — Defective U17, U13, U25

A STEP 13   Measure the BA signal on pin 26 of IC U17.
           • Result = +5 VDC Pulse   — Continue to 7. PCB REPLACEMENT.
           • Result = Incorrect   — Defective U17, U19, U27

7. PCB REPLACEMENT

There is no possible way to cover 100% of the problems that may arise internal to the C-64. The checks given in this manual basically cover problems where even the diagnostic does not produce a screen on system power-up. If the problem is not discovered during these checks:

PCB REPLACEMENT IS RECOMMENDED